Unified Exception Handling For Hierarchical Multi-Interrupt Architectures

ABSTRACT OF THE DISCLOSURE

A unified interrupt handling system and method is provided for an embeddable processor having multiple interrupt types. An instruction is inserted into the first vector address that disables the second interrupt mode. At the second vector address, an other instruction is inserted that branches to a common interrupt dispatcher. The common interrupt dispatcher is provided with an interrupt routine that processes the interrupt, and then re-enables the second interrupt modes. Interrupt requests are then processed by the common interrupt dispatcher without interruption.